IN THE CLAIMS

Please amend the claims as follows:

1. (PRESENTLY AMENDED) A common mode feedback circuit apparatus comprising:

a first and a second node defining a differential node pair; and

a collective plurality of transconductors including a first plurality of transconductors associated with the first node and a second plurality of transconductors associated with the second node, wherein at least one transconductor of the collective plurality has an adjustable transconductance, wherein ~~the~~ a total transconductance of each of the first and second pluralities is nominally halved between any adjustable transconductors and ~~the~~ remaining transconductors of that plurality.

2. (ORIGINAL) The apparatus of claim 1 wherein the total transconductance of each of the first and second pluralities is nominally halved between the set of transconductors capable of being decoupled from its associated node and recoupled to a complementary node and the remaining transconductors of that plurality.

3. (ORIGINAL) The apparatus of claim 1 wherein each of the first and second plurality of transconductors includes at least one transconductor with an adjustable transconductance.

4. (ORIGINAL) The apparatus of claim 3 further comprising:

a calibration engine, wherein while in a calibration mode the calibration engine varies each of the adjustable transconductances until a sensed differential voltage across the differential node pair is substantially zero.

5. (PRESENTLY AMENDED) The apparatus of claim 4 further comprising:

a calibration signal voltage source; and

a plurality of switches for switching between a calibration mode and a normal mode, wherein while in calibration mode the switches couple a common mode voltage signal from a common mode node to non-adjustable transconductors of the first and second pluralities, wherein the switches couple each of the adjustable transconductors to their complementary nodes, wherein the switches couple the calibration signal voltage source to the adjustable transconductors, wherein a current generated by the adjustable transconductors is proportional to the calibration signal voltage source, wherein the calibration signal voltage source is independent of the common mode voltage signal.

6. (ORIGINAL) The apparatus of claim 5 wherein while in normal mode the plurality of switches decouple the adjustable transconductors from the calibration signal voltage source, decouple the adjustable transconductors from their complementary nodes, and couple the adjustable transconductors to their respective associated differential nodes.

7. (ORIGINAL) The apparatus of claim 1 wherein each of the first plurality and second plurality comprises 2 transconductors.

8. (ORIGINAL) The apparatus of claim 7 wherein every transconductor of the collective plurality has substantially a same nominal transconductance value.

9. (ORIGINAL) The apparatus of claim 1 wherein the circuitry is implemented on an integrated circuit semiconductor die.

10. (ORIGINAL) The apparatus of claim 9 wherein the integrated circuit is a complementary metal oxide semiconductor (CMOS) integrated circuit.

11. (ORIGINAL) The apparatus of claim 1 further comprising:

a calibration engine, wherein the calibration engine varies the adjustable transconductance of the at least one transconductor until a sensed differential voltage across the differential node pair is substantially zero.

12. (ORIGINAL) The apparatus of claim 11 wherein the calibration engine further comprises a band pass filter to sense the differential voltage at a pre-determined frequency.

13. (ORIGINAL) A method of calibrating a common mode feedback block circuit, comprising the steps of:

a) providing a common mode feedback block apparatus having a first node and a second node forming a differential node pair, the apparatus further comprising a collective plurality of transconductors including a first plurality of transconductors associated with the first node and a second plurality of

transconductors associated with the second node, the collective plurality including at least one adjustable transconductor; and

b) adjusting the at least one adjustable transconductor until a differential voltage across the differential node pair is substantially zero.

14. (ORIGINAL) The method of claim 13 wherein step b) is performed while the common mode feedback block is in a calibration mode.

15. (ORIGINAL) The method of claim 13 wherein step b) further comprises the step of sensing the differential voltage only at a pre-determined frequency.

16. (ORIGINAL) The method of claim 13 further comprising the step of:

c) switching the common mode feedback block to a normal mode to prevent further transconductance adjustments to the at least one adjustable transconductor.

17. (ORIGINAL) The method of claim 13 wherein each of the first and second nodes has at least one associated adjustable transconductor, wherein step b) further includes the step of adjusting each of the associated adjustable transconductors until the differential voltage across the differential node pair is substantially zero.

18. (PRESENTLY AMENDED) The method of claim ~~14~~ 17 wherein the adjustable transconductors are adjusted by increasing a transconductance of a transconductor associated with the first node by an amount δ and decreasing a

transconductance of a transconductor associated with the second node by the amount δ.

19. (PRESENTLY AMENDED) The method of claim 13 further comprising the step of:

c) providing a calibration signal source independent of a common mode node, wherein during calibration the calibration signal source provides a control voltage for ~~the~~ any adjustable transconductor, ~~transconductors,~~ wherein the common mode node provides the control voltage for ~~the~~ remaining transconductors of the collective plurality of transconductors.

20. (ORIGINAL) The method of claim 19 wherein the calibration signal source and the common mode feedback block reside on a same integrated circuit die.